

1     1.     An apparatus for characterizing an insulating layer constructed between a  
2             conductive gate and a substrate, comprising:

3                     at least one test structure formed at a surface of a substrate, each  
4                     test structure comprising:

5                     a bulk region formed of a semiconductor within said surface,

6                     at least one source region within the bulk region,

7                     at least one drain region within the bulk region such that each  
8                     drain region is placed at a distance from one of the source  
9                     regions,

10                    a thin insulating layer placed above the each source region,  
11                    each drain region, and the bulk region between said source  
12                    region and said drain region, and

13                    the conductive gate placed above the thin insulating layer; and

14                    a capacitance-voltage measuring device having a sense probe in  
15                    contact the conductive gate of each test structure, a stimulus  
16                    probe in contact with the source and drain region of each test  
17                    structure to measure a capacitance value of said test structure,  
18                    and a bulk biasing probe to force said bulk region between said  
19                    source and drain region to a second voltage level, whereby said  
20                    second voltage level forces said bulk region to an inversion,

21                   said capacitance-voltage measuring device varying a first  
22                   voltage at said source and drain region to force said test  
23                   structure into the inversion state and measuring a first  
24                   capacitance of said test structure.

1    2.    The apparatus of claim 1 further comprising an insulating layer thickness  
2           calculator in communication with the capacitance-voltage measuring  
3           device to receive the capacitance as measured and from said capacitance  
4           determine the thickness of said insulating layer.

1    3.    The apparatus of claim 1 wherein the bulk biasing probe forces the bulk  
2           region to the second voltage level equal to said first voltage and said  
3           capacitance-voltage measuring device measures a second capacitance of  
4           said test structure, a parasitic capacitance of said test structure being a  
5           difference between the second capacitance and the first capacitance.

1    4.    The apparatus of claim 1 wherein the test structure has an area of less  
2           than  $10,000\mu\text{m}^2$ .

1    5.    The apparatus of claim 1 wherein the test structure has an area of less  
2           than  $1,000\mu\text{m}^2$ .

1    6.    The apparatus of claim 1 wherein the insulating layer thickness is less  
2           than  $22\text{\AA}$ .

1     7.     A apparatus for determining thickness of an insulating layer constructed  
2           between a conductive gate and a substrate, comprising:

3                     at least one test structure formed at a surface of a substrate, each  
4                     test structure comprising:

5                     a bulk region formed of a semiconductor within said surface,  
6                     at least one source region within the bulk region,  
7                     at least one drain region within the bulk region such that each  
8                     drain region is placed at a distance from one of the source  
9                     regions,

10                    a thin insulating layer placed above the each source region,  
11                    each drain region, and the bulk region between said source  
12                    region and said drain region, and

13                    the conductive gate placed above the thin insulating layer;

14                    a capacitance-voltage measuring device having a sense probe in  
15                    contact the source region and the drain region of each test  
16                    structure, a stimulus probe in contact with the source and drain  
17                    region of each test structure to measure a capacitance value of  
18                    said test structure, and a bulk biasing probe to force said bulk  
19                    region between said source and drain region, said capacitance-  
20                    voltage measuring device varying a first voltage level between

21                   said stimulus probe and said sense probe said bulk biasing  
22                   probe to a second voltage level to force said test structure into  
23                   an inversion state and measuring a first capacitance of said test  
24                   structure; and

25                   an insulating layer thickness calculator in communication with the  
26                   capacitance-voltage measuring device to receive the  
27                   capacitance as measured and from said capacitance,  
28                   determines the thickness of said insulating layer.

1    8.    The apparatus of claim 7 wherein the bulk biasing probe forces the bulk  
2           region to the second voltage level to be equal to said first voltage and said  
3           capacitance-voltage measuring device measures a second capacitance of  
4           said test structure, a parasitic capacitance of said test structure being a  
5           difference between the second capacitance and the first capacitance.

1    9.    The apparatus of claim 7 wherein the test structure has an area of less  
2           than 10,000 $\mu\text{m}^2$ .

3    10.   The apparatus of claim 7 wherein the test structure has an area of less  
4           than 1,000 $\mu\text{m}^2$ .

1    11.   The apparatus of claim 1 wherein the insulating layer thickness is less  
2           than 22Å.

1     12.     A method for characterizing an insulating layer constructed between a  
2             conductive gate and a substrate, comprising the steps of:

3                     forming at least one test structure at a surface of a substrate by the  
4                     steps of:

5                     forming a bulk region of a semiconductor within said surface,  
6                     creating at least one source region within the bulk region,  
7                     creating at least one drain region within the bulk region such  
8                     that each drain region is placed at a distance from one of the  
9                     source regions,

10                    constructing a thin insulating layer above the each source  
11                    region, each drain region, and the bulk region between said  
12                    source region and said drain region, and

13                    placing the conductive gate above the thin insulating layer; and

14                    performing a capacitance-voltage measurement by the steps of:

15                    connecting the source region with the drain region of each test  
16                    structure,

17                    placing a sense probe in contact the conductive gate of each  
18                    test structure,

19 placing a stimulus probe in contact with the source and drain  
20 region of each test structure to measure a capacitance value  
21 of said test structure,  
  
22 varying a first voltage between said stimulus probe and said  
23 sense probe to force said test structure into an inversion  
24 state,  
  
25 placing a bulk biasing probe in contact with said bulk region to  
26 force said bulk region between said source and drain region  
27 to a second voltage to insure said inversion state,, and  
  
28 measuring a first capacitance of said test structure.

1 13. The method of claim 13 further comprising the step of:

2 determining the thickness of said insulating layer from said first  
3 capacitance.

1 14. The method of claim 13 further comprising the steps of:

2 forcing the bulk region the second voltage level equal to said first  
3 voltage, and

4 measuring a second capacitance of said test structure,

5                   calculating a parasitic capacitance of said test structure as a  
6                   difference between the second capacitance and the first  
7                   capacitance.

1    15.    The method of claim 13 wherein the test structure has an area of less than  
2           10,000 $\mu\text{m}^2$ .

1    16.    The method of claim 13 wherein the test structure has an area of less than  
2           1,000 $\mu\text{m}^2$ .

1    17.    The method of claim 13 wherein the insulating layer thickness is less than  
2           22Å.

1    18.    A method for determining thickness of an insulating layer constructed  
2           between a conductive gate and a substrate, comprising the steps of:

3                   forming at least one test structure at a surface of a substrate by the  
4                   steps of:

5                   forming a bulk region of a semiconductor within said surface,

6                   creating at least one source region within the bulk region,

7                   creating at least one drain region within the bulk region such

8                   that each drain region is placed at a distance from one of the  
9                   source regions,

10                   constructing a thin insulating layer above the each source  
11                   region, each drain region, and the bulk region between said  
12                   source region and said drain region, and  
  
13                   placing the conductive gate above the thin insulating layer; and  
  
14                   performing a capacitance-voltage measurement by the steps of:  
  
15                   connecting the source region with the drain region of each test  
16                   structure,  
  
17                   placing a sense probe in contact the conductive gate of each  
18                   test structure,  
  
19                   placing a stimulus probe in contact with the source and drain  
20                   region of each test structure to measure a capacitance value  
21                   of said test structure, and  
  
22                   placing a bulk biasing probe in contact with said bulk region  
23                   between said source and drain region,  
  
24                   varying a first voltage at said source and drain region to force  
25                   said test structure into an inversion state,  
  
26                   forcing said bulk region to a second voltage to insure said  
27                   inversion state, and  
  
28                   measuring a first capacitance of said test structure; and



29 determining the thickness of said insulating layer from said first  
30 capacitance.

1 19. The method of claim 18 further comprising the steps of:

2 forcing the bulk region to a second voltage level equal to said first  
3 voltage, and

4 measuring a second capacitance of said test structure,

5 calculating a parasitic capacitance of said test structure as a  
6 difference between the second capacitance and the first  
7 capacitance.

1 20. The method of claim 18 wherein the test structure has an area of less than  
2  $10,000\mu\text{m}^2$ .

1 21. The method of claim 18 wherein the test structure has an area of less than  
2  $1,000\mu\text{m}^2$ .

1 22. The method of claim 18 wherein the insulating layer thickness is less than  
2  $22\text{\AA}$ .

1 23. A method for measuring capacitance-voltage curves for a transistor,  
2 comprising the steps of:

3 providing a substrate having a well area having at least one  
4 isolation region and a well pick-up contact therein and the  
5 transistor thereon,  
6 said transistor comprising a gate, a gate dielectric, and  
7 source/drain regions;  
8 measuring a first capacitance-voltage curve of the transistor under  
9 inversion and accumulation conditions by the step of:  
10 applying a direct current signal and an alternating current signal  
11 between the gate and a common connection of the  
12 source/drain regions and the well pick-up contact; and  
13 measuring a second capacitance-voltage curve of the transistor  
14 under inversion conditions by the steps of:  
15 applying the direct current signal and the alternating current  
16 signal between the gate and the source/drain regions, and  
17 floating the well pick-up contact.

1 24. The method of claim 23, further comprising the step of:  
2 determining a parasitic capacitance by the step of:  
3 obtaining a capacitance difference between the first and second  
4 capacitance-voltage curves under inversion condition.

1     25.     The method of claim 24, further comprising the step of:

2                     determining the second capacitance-voltage curve under the  
3                     accumulation condition by the difference between the first  
4                     capacitance-voltage curve under the accumulation condition  
5                     and the capacitance difference.

1     26.     A method of measuring capacitance-voltage curves for a transistor,  
2             comprising the steps of:

3                     providing a substrate having a well area having at least one  
4                     isolation region and a well pick-up contact therein and the  
5                     transistor thereon,

6                     said transistor comprising a gate, a gate dielectric, and  
7                     source/drain regions;

8                     measuring a first capacitance-voltage curve of the transistor under  
9                     inversion and accumulation conditions by the step of:

10                    applying a direct current signal and an alternating current signal  
11                    between the gate and a common connection of the  
12                    source/drain regions and the well pick-up contact; and

13                    measuring a second capacitance-voltage curve of the transistor  
14                    under inversion conditions by the steps of:

15                   applying the direct current signal and the alternating current  
16                   signal between the gate and the source/drain regions, and  
17                   applying a second direct current signal to the well pick-up.

1    27.    The method of claim 26, further comprising the step of:

2                   determining a parasitic capacitance by the step of:

3                   obtaining a capacitance difference between the first and second  
4                   capacitance voltage curves under inversion condition.

1    28.    The method of claim 27, further comprising the step of:

2                   determining the second capacitance-voltage curve under the  
3                   accumulation condition by the difference between the first  
4                   capacitance-voltage curve under the accumulation condition  
5                   and the capacitance difference.

1    29.    A method of measuring capacitance-voltage curves for a MOS transistor,  
2            comprising the steps of:

3                   providing a substrate having a well area having at least one  
4                   isolation region and a well pick-up contact therein and the MOS  
5                   transistor thereon,

6                   measuring a first capacitance-voltage curve of the MOS transistor  
7                   under inversion and accumulation conditions by the step of:

8                   applying a direct current signal and an alternating current signal  
9                   between a gate of said MOS transistor and a common  
10                  connection of source/drain regions of said MOS transistor  
11                  and the well pick-up contact; and

12                measuring a second capacitance-voltage curve of the MOS  
13                transistor under inversion conditions by the steps of:

14                applying the direct current signal and the alternating current  
15                signal between the gate and the source/drain regions, and  
16                floating the well pick-up contact.

1    30.    The method of claim 29, further comprising the step of:

2                determining a parasitic capacitance by the step of:

3                obtaining a capacitance difference between the first and second  
4                capacitance-voltage curves under inversion condition.

1    31.    The method of claim 30, further comprising the step of:

2                determining the second capacitance-voltage curve under the  
3                accumulation condition by the difference between the first  
4                capacitance-voltage curve under the accumulation condition  
5                and the capacitance difference.

1     32.     An apparatus for measuring capacitance-voltage curves for a transistor,  
2             which comprises a well pick-up contact, a gate, and source/drain regions,  
3             comprising:  
  
4                 a measuring unit connected to said transistor  
  
5                 for measuring a first capacitance-voltage curve of the transistor  
6                 under inversion and accumulation conditions by connecting  
7                 the gate and the source/drain regions and the well pick-up  
8                 contact for applying a direct current signal and an alternating  
9                 current signal between the gate and the source/drain  
10                regions, and  
  
11               for measuring a second capacitance-voltage curve of the  
12               transistor under inversion conditions by connecting the gate  
13               and the source/drain regions for the direct current signal and  
14               the alternating current signal are applied between two  
15               terminals and floating the well pick-up contact; and  
  
16               a characteristic calculating unit coupled to the measuring unit for  
17               obtaining the first and second capacitance-voltage curves under  
18               and calculating a parasitic capacitance as a capacitance  
19               difference between the first and second capacitance-voltage  
20               curves under inversion condition and for determining the second  
21               capacitance-voltage curve under the accumulation condition by

22                   the difference between the first capacitance-voltage curve under  
23                   the accumulation condition and the parasitic capacitance.